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A Complete CMOS UWB Timed-Array Transmitter with a 3D Vivaldi Antenna Array for Electronic High-resolution Beam Spatial Scanning

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Abstract—We present a new Ultra Wide Band (UWB) Timed-Array Transmitter System with Beamforming capability for high-resolution remote acquisition of vital signals. The system consists of four identical channels, where each one is formed of a serial topology with three modules: programmable delay circuit (PDC or $\tau$), a novel UWB 5\textsuperscript{th} Gaussian Derivative order pulse generator circuit (PG), and a planar Vivaldi antenna. The circuit was designed using 0.18\textmu m CMOS standard process and the planar antenna array was designed with film-conductor on Rogers RO3206 substrate. Spice simulations results showed the pulse generation with 104 mVpp amplitude and 500 ps width. The power consumption is 543 $\mu$W, and energy consumption 0.27 pJ per pulse using a 2V power supply at a pulse repetition rate (PRR) of 100 MHz. Electromagnetic simulations results, using CST Microwave (MW) Studio 2011, showed the main lobe radiation with a gain maximum of 13.2 dB, 35.5° x 36.7° angular width, and a beam steering between 17° and -11° for azimuthal ($\phi$) angles and 17° and -18° for elevation ($\theta$) angles at the center frequency of 6 GHz.

Health monitoring; respiration rate; beamforming; timed array; UWB; heartbeat signal;

I. INTRODUCTION

Currently, there is considerable research being conducted on UWB radars, mainly (but not only) for application in the remote acquisition of heartbeat signals or the measurement of respiration rate (e.g. a group of soldiers in a military vehicle or workers in a nuclear power plant). Moreover, UWB radars promise good performance for other of military or civil applications (e.g. as ground and wall penetrating, victim localizations in the rubble of a landslide or snow, in pediatric clinics for alerting and monitoring of the Sudden Infant Death Syndrome (SIDS), or biomedical imaging) [1-6]. This technique is formed for a transmitter (this work) and a receiver to perform telemetry and estimating the vital signs through detection of the motion of lung and heart walls.

The case of vital signs acquisition requires a high precision system that can capture the signals of each individual dynamically, as this type of analysis in motion can cause significant changes in waveform on the radiated UWB pulse [1, 6, 7]. With this objective, it is essential to use a radar system equipped with high-gain directional antennas to minimize reflections from the environment [7], justifying the choice of a beamforming system.

Another important point is to ensure the coexistence with other systems, and for this, being spread in an ultra-wide frequency range the spectral power of the pulses, minimizing the likelihood of interference with other communication systems, such as cell phones (e.g. GSM900, and UMTS/WCDMA), GPS, Bluetooth, and W-LAN IEEE 802.11 [8, 9].

Figure 1 shows the proposed timed-array transmitter system, formed by four identical channels, each one composed by a PDC, a PG, and a Vivaldi antenna, mounted in a dual cross antenna array (2+2), proposed by [5], so as to permit spatial (3D) beam steering.

The work is organized as follows: in Sec II, the transmitter circuit and antenna array architecture and design are presented. Also the results of electromagnetic simulation in CST MW 2011[12], along with the results of Spice simulations, are presented in Sec III, and the conclusions are covered in Sec IV. The integrated system simulations with MicroWind 3.5[10] combined with LTSpice 4[11] for layout and schematic, where effects of crosstalk coupling vertical and horizontal, input noise of 10 mVpp and parameters variation (voltage, temperature, geometrical dimensions w and l) of the +/- 20% were considered by Monte-Carlo MOS level 3, with unknowns values are randomly selected according with their statistical distribution.

II. SYSTEM BEAMFORMING ARCHITECTURE OVERVIEW

A radar system based on timed-array, as well as phased-array, avoids the use of complicated mechanical systems, (mechanical scanning radar). In contrast to phased-array system that only operates with carrier signal, the timed-array system operates with discrete pulses (carrier free) and may have a pattern of different spacing between the antennas [1, 5, 13, 14], e.g. when the antennas are excited with a delay time of 0 ps for channels 1 and 2, and of 63 ps for channels...
Each block of the transmitter is explained, including the antenna array in the next sections.

A. Programmable delay array – PDC

The PDC presented in this paper is based on investigations from [5], which resulted in a PDC with a waveform delay quasi-linear, in contrast to the PDC presented in a previous work [1], whose delay waveform (delay vs. control word) was non-linear. Fig. 2(a) shows the PDC-array architecture.

The circuit consists of four independent channels, with details shown in Fig. 2(b), and each one is formed by two inverters, connected in series, with a variable resistor (Fig. 2(c)) between the transistor Mn4 (the first nMOS inverter) and Vss. The time propagation is dependent on the discharge time of Mn2 transistor gate capacitance of, and is changed in function of the variable resistor. Therefore the system provides a controlled delay.

According to the investigations in [5], it is possible to obtain a PDC with the series combination of two inverters and by controlling the capacitive or resistive properties of the circuit. The work presented in [1] accomplished the delay control using a digital capacitor, resulting in a nonlinear waveform delays. The present investigation used a variable resistor to obtain a quasi-linear waveform delay, as shown in Fig. 3(a).

Figure 3 shows the nonlinearity of the PDC from [1] vs. the quasi-linearity of the proposed PDC, for the control words (4, 8, 9, and 12), as viewed in shadow areas in item (b) of the figure.

B. The New 5th derivative Gaussian pulse generator

There are several pulses that can be used in UWB applications [5]. The Sinc pulse is considered the most suitable one, by presenting a lower rate of lateral spread, but it is complex to synthesize it. On the other hand, the rectangular pulse is easily generated, but has considerable lateral spreading.

Another option is to use the Gaussian pulse, although it presents a DC component (zero frequency), which makes its electromagnetic emission less efficient, and does not meet the requirements set by the Federal Communication Commission (FCC) [5,15]. As a result, the use of Gaussian derivative pulse in the 5th order was suggested [5], since it presents no DC component, has a lower rate of lateral spreading and meets the FCC requirements.

According to the investigations in [5], it is possible to obtain a PDC with the series combination of two inverters and by controlling the capacitive or resistive properties of the circuit. The work presented in [1] accomplished the delay control using a digital capacitor, resulting in a nonlinear waveform delays. The present investigation used a variable resistor to obtain a quasi-linear waveform delay, as shown in Fig. 3(a).

Figure 3 shows the nonlinearity of the PDC from [1] vs. the quasi-linearity of the proposed PDC, for the control words (4, 8, 9, and 12), as viewed in shadow areas in item (b) of the figure.

Figure 2. General PDC array structure: (a) PDC array; (b) PDC Unit; (c) Digital Variable Resistor Circuit.

Figure 4. The proposed 5th derivative Gaussian PG: (a) general structure of the PG; (b) Simplified time diagram; (c) PG proposed in [16,17]; (d) AND gate formed by a pseudo nMOS NAND gate and a static inverter; (e) Static inverter circuit; and (f) three inverter delay circuit.

The novel system architecture is illustrated in Fig. 4(a). It consists of two identical static inverters in series. They transform the arbitrary input signal Vin into a square waveform Vtrig (Vtrg). Next, there is a triangular pulse generator [5,16,17], responsible for the generation of a triangular pulse that is inverted by the static inverter (Vd). This inverted triangular pulse is later spread and inverted by the delay line (Vb, Vc, Vd, Vf, and Vf), each time the wave excites the pulse shape transistors (M11p, M14n, M12p, M15n, M13p, and M16n). The current that passes through the C capacitor (570 Ωf) blocks out the DC component, and also generates the Vout signal that is shaped according to the 5th derivative of the Gaussian pulse, shown in Fig. 4(b).

A 50Ω load impedance is used in the circuit during the electrical simulations, in order to simulate a realistic antenna. After obtaining the output pulse, it was exported to the CST MW 2011, which was used to simulate the antenna, and thus generate the integration in both environments. This
procedure was executed in order to meet the FCC regulations for UWB systems, which require that the output pulse should be obtained from the complete system, including the transmitter and antenna. For the final IC design however, this impedance load was removed.

Each subsystem is described below:

1) Square-wave rectifier

This subsystem consists of two identical static inverters used to rectify time-varying waveforms such as square waves, following the proposed pulse generator presented in [18]. The inverter architecture is illustrated in Fig. 4(e), which consists of a pMOS (M25p with \(w=4\) \(\mu m\) and \(l=0.2\) \(\mu m\), with \(I_{\text{max}}=946\) \(\mu A\)) and a nMOS (M26n with \(w=2\) \(\mu m\) and \(l=0.2\) \(\mu m\), with \(I_{\text{max}}=1185\) \(\mu A\)) transistors, operating as switches. When the input signal has a low level (\(Vss\)), the nMOS gate is reversely biased while the pMOS gate is directly biased, therefore generating a high level (\(Vdd\)) at its output. Conversely, a high level signal is applied in the input generates a low level (\(Vss\)) at the output.

Since the Monte Carlo average response time of the proposed inverter is in the range of 40 ps (7.5 times faster compared to the transition from a sine wave of same frequency), the connection of two inverters in series conforms the input time-varying signal into a square wave. The same inverter is used in the output of the triangular pulse.

2) Triangle pulse generator

The triangular pulse generator, Fig. 4 (c), used in this work is based on the Glitch generator proposed by Rabaey in [16] and was firstly used for generating triangular UWB pulses circuit by Zhang [17] and more recently by De Oliveira [5].

The triangle pulse generator was developed around a simple feedback network and an AND gate (Fig. 4 (d)).

The architecture of the triangle pulse generator is detailed in Fig. 4(c). At the time \(V_{\text{trigger}}\) is held at a low level (\(Vss\)), the AND gate (Fig. 4 (d)) output is at low level, so the nMOS transistor M18n (with \(w=1\) \(\mu m\) and \(l=0.2\) \(\mu m\), with \(I_{\text{max}}=58\mu A\)) is off. The capacitor \(C_x\) (via capacitance, gate capacitance of transistor M24n, and drain capacitance of transistors M17 and M18n) of the 15 IF is then charged to \(Vdd\) by the pMOS transistor M17p (with \(w=4\) \(\mu m\) and \(l=0.2\) \(\mu m\), with \(I_{\text{max}}=946\) \(\mu A\)). When the \(V_{\text{trigger}}\) signal reaches the high level (\(Vdd\)), M17p is immediately turned off and the AND gate output reaches a high level after a short gate delay \(\tau_{\text{AND}}\). Therefore, M18n is turned on to discharge the capacitor \(C_x\). When the signal \(Vx\) is changed to a level below the threshold voltage of the AND gate \(V_{\text{AND}}\), the AND gate output changes to a low level again after \(T\), thereby a triangular pulse (\(V_{\text{pulse}}\)) is produced.

3) Delay circuit

The delay circuit is composed of five delay cells, each one formed by three sets of identical static inverters. In Fig. 4(f), each inverter consists of the nMOS and pMOS transistors, for the first inverter they are M30n (with \(w=2\) \(\mu m\) and \(l=0.2\) \(\mu m\), with \(I_{\text{max}}=1144\) \(\mu A\)) and M27p (with \(w=4\) \(\mu m\) and \(l=0.2\) \(\mu m\), with \(I_{\text{max}}=898\) \(\mu A\)), respectively.

The delay time depends on the transistor channel dimensions; on the parasitic capacitances and on the number of inverters in the delay line. This particular setting for the delay circuit was chosen because of its simplicity and compact topology. The output of each delay cell is \(Vb, Vc, Vd, Ve\), and \(Vf\). Fig. 5 shows \(V_{\text{pulse}}\) and the other triangle waves that excite the transistors forming the pulse shaping stage.

![Waveform of the triangular pulses starting with the \(V_{\text{pulse}}\), and \(Vb\) signals, followed by delay cells output pulses \(Vb, Vc, Vd, Ve\), and \(Vf\).](image)

Figure 5. Waveform of the triangular pulses starting with the \(V_{\text{pulse}}\), and \(Vb\) signals, followed by delay cells output pulses \(Vb, Vc, Vd, Ve\), and \(Vf\).

4) Pulse shaping stage

The development technique of the pulse shaping stage presented in this paper is based on [1, 18], for UWB pulse generation seen in Fig. 6(a).

The pulse shaping stage consist of three charge-pumps, and each consists of two transistors, a pMOS and a nMOS, M11p (with \(w=0.6\) \(\mu m\) and \(l=0.2\) \(\mu m\), with \(I_{\text{max}}=127\mu A\)) generating the first peak of the pulse with 7 \(mV\), and M14n (with \(w=1.2\) \(\mu m\) and \(l=0.2\) \(\mu m\), with \(I_{\text{max}}=677\mu A\)) generating the first valley pulse with -30 \(mV\) (for first charge-pump), M12p (with \(w=5\) \(\mu m\) and \(l=0.2\) \(\mu m\), with \(I_{\text{max}}=1124\mu A\)) generating the second peak of the pulse with 50\(mV\) and M15n (with \(w=2.8\) \(\mu m\) and \(l=0.2\) \(\mu m\), with \(I_{\text{max}}=1610\mu A\)) generating the second valley pulse with -54\(mV\) (second charge-pump), and M13p (with \(w=2.2\) \(\mu m\) and \(l=0.2\) \(\mu m\), with \(I_{\text{max}}=490\mu A\)) generating the third peak of the pulse with 26 \(mV\) and M16n (with \(w=0.6\) \(\mu m\) and \(l=0.2\) \(\mu m\), with \(I_{\text{max}}=327\mu A\)) generating the third valley pulse with -15 \(mV\) (last charge-pump), as shown in Fig. 4(a) and Fig. 6(a).

It is observed that the charge-pump output currents are controlled and combined successively by these transistors. As a result, a fifth derivative Gaussian pulse is generated, illustrated in Fig. 4(b), with its waveform in Fig. 6(a), and output pulse magnitude \(Vout\) is controlled by the charge-pumps output transistors. The transistor sizes are chosen based on the required amplification level to shape the output UWB waveform [1,18].

5) Pulse generator simulation results

The simulation of the proposed UWB pulse generator using Spice shows that the circuit can be robustly operated, in other words, showing the 5th Gaussian pulse waveform at \(Vout\) unchanged with 20\% variation of the parameters in Monte Carlo simulations (varying supply voltage, geometry, temperature and input noise).

The simulation results showed that the fifth-order derivative Gaussian pulse is similar to the calculated theoretical pulse, as seen in Fig. 6(a), with the simulated pulse indicated in solid line and the normalized theoretical pulse shown by the dotted line. The amplitude of the
simulated pulse is 104 mVpp and its pulse width has 500 ps. The average power consumption was 543 µW and energy consumption of 271 fJ per pulse is found at input PRR’s of 100 MHz and 2 V power supply, with a bandwidth of 5.26 GHz (level between -50.3 dBm and -40.3 dBm) showed in detail in Fig. 6(b).

The consumption is lower than that in the system of [19,20]. Table I shows a comparison between this pulse generator and various previously reported designs in the literature, the new topology here proposed can transmit an UWB pulse with higher energy efficiency, which contributes to increased the battery lifetime.

<table>
<thead>
<tr>
<th>Parameters/References</th>
<th>This work</th>
<th>[1]</th>
<th>[19]</th>
<th>[20]</th>
<th>[21]</th>
<th>[22]</th>
<th>[23]</th>
<th>[24]</th>
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<tr>
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<td>7th</td>
<td>7th</td>
<td>5th</td>
<td>5th</td>
<td>2nd</td>
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<td>Multi</td>
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<td>180</td>
<td>180</td>
<td>500</td>
<td>180</td>
<td>180</td>
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<td>1.8</td>
<td>5</td>
<td>--</td>
<td>1.8</td>
<td>--</td>
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<tr>
<td>PRR (MHz)</td>
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<td>100</td>
<td>1</td>
<td>--</td>
<td>--</td>
<td>1160</td>
<td>--</td>
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<tr>
<td>Pulse duration (ps)</td>
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<td>350</td>
<td>800</td>
<td>380</td>
<td>240</td>
<td>999</td>
<td>280</td>
<td>2000</td>
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<tr>
<td>Ampl. (mVpp)</td>
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<td>136</td>
<td>500</td>
<td>700</td>
<td>148</td>
<td>30</td>
<td>123</td>
<td>900</td>
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<tr>
<td>Energy consum./ pulse (pJ)</td>
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<td>0.4</td>
<td>4.7</td>
<td>--</td>
<td>58</td>
<td>--</td>
<td>--</td>
<td>180</td>
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<tr>
<td>Power consum./ pulse (mW)</td>
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<td>--</td>
<td>--</td>
<td>--</td>
<td>21</td>
<td>12.6</td>
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</table>

Table II summarizes the global performance of the proposed UWB pulse generator.

### Table II. Summary of the Simulated Pulse Generator Performance.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Results</th>
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<tbody>
<tr>
<td>Bandwidth</td>
<td>5.26 GHz</td>
</tr>
<tr>
<td>Sub-band center frequency</td>
<td>6 GHz</td>
</tr>
<tr>
<td>Peak PSD</td>
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<tr>
<td>Pulse Amplitude</td>
<td>104 mVpp</td>
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<tr>
<td>Pulse duration</td>
<td>500 ps</td>
</tr>
<tr>
<td>Energy consumption p/pulse</td>
<td>0.27 pJ</td>
</tr>
<tr>
<td>Power consumption p/pulse</td>
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<tr>
<td>Power supply</td>
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</tr>
<tr>
<td>Pulse repetition rate</td>
<td>100 MHz</td>
</tr>
<tr>
<td>Technology</td>
<td>180 nm</td>
</tr>
</tbody>
</table>

6) Proposed Layout

Fig. 7 shows the proposed UWB pulse generator circuit layout, without pads, with the input signal ($V_{pca}$), square-wave rectifier, the triangular pulse generator, the delay cells, and the pulse shaping circuit. Guard rings are used to minimize latch-up effects and interference between adjacent circuits. The complete pulse generator circuit occupies an area of 26x33µm², without pads.

C. Vivaldi antenna array

A 2+2 array of Antipodal Vivaldi antennas is proposed for the beamforming. The Vivaldi antennas, belong to the class of continuously scaled, aperiodic, and exponential curved antennas. Theoretically this antenna has a constant beamwidth at unlimited operating frequency range, therefore suitable for UWB applications [26, 27, 28].

The substrate used is the Rogers RO3206 (with a relative dielectric constant of 6.15). The opening exponential taper of the antenna is responsible for its large bandwidth, as described in [26].
In contrast to narrowband phased array systems, which have as a requirement the distance between array elements of $\lambda/2$ fixed, the proposed UWB timed array provides greater design freedom regarding the distance between the elements [13]. The distance between the elements (d) of array proposed in this paper was used as the design parameter and varied 36.3 mm, which corresponds 5/7 of $\lambda$ at 6 GHz to 72.6 mm, corresponding to 1 and 4/9 of $\lambda$ at 6 GHz.

The gain of the arrangement with $d = 36.3$ mm showed two problems; it was not uniform between frequencies from 5 to 7 GHz, and possessed 4.5 dB and 9.2 dB as lower and upper gain limits, whereas with $d = 72.6$ mm it resulted in a higher and uniform gain, ranging from 9.2 to 13.5 dB as lower and upper gain limits, although this arrangement occupies a volume 200% larger than the previous arrangement. The chosen space between these two values is $d = 58.1$ mm, which shows good uniformity in gain over the 5 to 7 GHz range with upper and lower limits of 8 to 13.2 dB gain and a volume occupying only 108% higher.

Figure 9 shows the gain versus frequency for the beam with the following control PDC-array words: \{0000h, F000h, 0F00h, 00F0h, 000Fh\}, with $d$ equal to \{36.3, 58.1, 72.6 mm\}. The main lobe direction is given by the relationship between the $\Delta\tau$, which is propagation delay between the antennas set by the PDC, the distance ($d$) between the antennas, and the light speed ($c$), as follows:

$$\theta = \arcsin\left(\frac{\Delta\tau \cdot c}{d}\right)$$  \hspace{1cm} (1)

for azimuthally angles and,

$$\varphi = \arcsin\left(\frac{\Delta\tau \cdot c}{d}\right)$$  \hspace{1cm} (2)

for elevation angles.

### III. SIMULATION RESULTS

The simulation of the pulse beamforming transmitter in the Spice environment shows a pulse amplitude of 104 mVpp and 500 ps of pulse width, as well as a main lobe with an average gain of 13.1 dB, 35.5° x 36.7° angular width and a beam steering between 17° x -11° to the $\theta$ angle and between 17° and -18° to the $\varphi$ angles for maximum values.

Table IV and Fig. 10 show some possibilities for beamforming alongside with the required configuration parameters. The first to fourth column are the PDC control words, in hexadecimal base; the fifth and eighth column contain the corresponding time delays in ps; and, finally, the ninth and eleventh columns are of the parameters of the beam steering and the respective gain results.

### IV. CONCLUSION

This paper presents the design of a new timed array UWB transmitter pulse generator system with beamforming capability composed of CMOS 0.18 µm standard technology, as well as an 3D antenna array design integrated with Spice and CST 2011 MW. The simulation results showed a controllable beam steering between 17° and -11° for $\theta$ angles and between 17° and -18° for $\varphi$ angles with a maximum gain of 13.2 dB. This control was achieved using a PDC array circuit that can generate delays digitally controlled from 0 to 63 ps. The pulses obtained resulted in a signal with 104mVpp amplitude and 500ps of pulse duration and a power consumption of 543μW, and energy consumption of 0.27pJ per pulse using 2V power supply at PPR of 100MHz.
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