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Trapezoidal cross-sectional influence on FinFET threshold voltage and corner effects

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In recent years, the downscaling of complementary metal-oxide semiconductor (CMOS) device dimensions as well as some mobility-improving techniques such as strained silicon have been the preferred solutions for achieving the necessary performance evolution for the growth of the microelectronics industry. Some alternative solutions have extended the possibility of scaling devices beyond the fundamental physical limits of bulk MOS transistors. The silicon-on-insulator (SOI) technology has been an extremely attractive solution in terms of performance and scalability. The short-channel effects are remarkably reduced in thin SOI films compared to bulk silicon. From the experience of having the best control of inversion charge by back and front gates of fully depleted SOI devices, the idea of multiple-gate devices has been developed. A direct application of this idea is the double-gate MOS field-effect transistor (FinFET), which has several architectural approaches addressing its theory and, mainly, its technological feasibility. These multiple-gate devices have introduced the concept of volume inversion; the minority carriers are spread out across the silicon film and not concentrated near the surface. The FinFET architecture is one possible approach to multiple-gate devices. Figure 1 shows a perspective view of a double-gate FinFET device. It is a quasi-planar device with vertical channel, and its fabrication process does not differ significantly from the traditional SOI-CMOS process.

**Triple-Gate FinFETs**

FinFETs can also be implemented as triple-gate structures, because the top oxide can be thin enough to act as a top gate oxide. Triple-gate FinFETs differ significantly from double-gate FinFETs in some aspects. First, the top-gate surface may have a different crystal-plane orientation from the lateral-gate surfaces. This fact implies different surface mobilities as well as different oxidation rates. During fabrication, greater oxidation rates lead to thicker gate oxides.

Another identified phenomenon caused by the presence of the top gate is the corner effect, which occurs due to the overlapping of the influences of two gate planes near the device corners. The corner effect is characterized by the increase of inversion charge in the proximity of the corners, with immediate consequences to current-density distribution along the fin cross section. Figure 2 shows the cross section of a simulated triple-gate device and some electron-concentration level curves. A greater carrier concentration can be clearly seen near the top corners. A similar effect occurs at the bottom corners, depending on the substrate bias, due to the influence of substrate potential and the gate bottom edge. The curves were obtained from an Atlas numeric simulator using the Bohm quantum potential (BQP) model. BQP is implemented in the Atlas numeric simulator as a way to consider the effects due to confinement of carriers in small-geometry FETs. The simulated device has a silicon height $H_{Si}$ of 50 nm, gate work function of 4.63 V, gate-oxide thickness $t_{ox}$ of 2 nm, buried-oxide thickness $t_{bur}$ of 100 nm, gate width $W_{Fin}$ of 50 nm, and gate length $L = 60$ nm. The device was biased with drain-to-source voltage $V_{DS} = 0.05$ V, gate-to-source voltage $V_{GF} = 0.42$ V (threshold voltage), and 0 V was the voltage applied below the buried oxide.

**Nonrectangular Cross Sections**

As a consequence of the limitations of process uniformity, most fabricated FinFETs present width variation along the vertical direction. Hard-mask geometry transfer and nonideal anisotropic overetch can result in trapezoid or triangular fin structures. The etching process can also cause more irregular shapes, such as convex or concave sidewall structures. In Ref. 9, the author presents some fin shapes from different references. Figure 3 shows these shapes for triple-gate FinFETs. The impact of a nonvertical sidewall on the threshold voltage and on the corner effects of FinFETs has been analyzed through three-dimensional simulation. Several double-gate and triple-gate devices of different doping levels, fin widths, and sidewall inclination angles were simulated, and the results are presented in this paper. Although the present work specifically addresses directly trapezoidal-shaped FinFET devices, the results may be extended to other nonvertical sidewall cross-sectional shapes.

**Threshold Voltage Analysis**

The threshold voltage is extracted directly from the drain current ($I_D$) vs gate voltage ($V_{G}$) curve of the simulated devices using the maximum transconductance change (MTC) method. The MTC...
Device simulator v. 5.10 was used.

Threshold voltage of triple-gate devices may be influenced by the corner effects, because inversion occurs in the corners at lower gate voltages than in the rest of the device. Some devices present more than one peak at the second derivative of the drain-current curve, and others present a diffuse maximum with no definite peak. Triple-gate FinFETs may also present different threshold voltages for the top and lateral gates, due to diverse gate-oxide widths, caused by top and lateral different crystal orientations. For these reasons, the analysis of the sidewall inclination angle on the threshold voltage was done using double-gate devices.

Figure 4 shows a double-gate FinFET in perspective. The simulated devices present gate-oxide thickness $t_{ox} = 3$ nm, buried-oxide thickness $t_{box} = 200$ nm, top silicon film width ($W_{Fin\ top}$) ranging from 10 to 50 nm, bottom silicon film width ($W_{Fin\ bottom}$) of 50 nm, silicon doping concentration ($N_d$) ranging from $10^{15}$ to $2.5 \times 10^{17}$ cm$^{-3}$, and interface charge densities of $3.0 \times 10^{10}$ cm$^{-2}$. The gate is implemented with a midgap material. Fin height ($H_{Fin}$) is 100 nm for all devices. The inclination angle $\theta$ ranges from 0 to 11.3°. The channel length ($L$) varies from 200 to 400 nm. The Atlas device simulator v. 5.10 was used.

Figure 5 presents the second derivative of the drain current as a function of the gate voltage for $\theta$ ranging from 0 to $\pi$ degrees, channel length 400 nm, and doping concentrations of $10^{15}$, $10^{16}$, and $10^{17}$ cm$^{-3}$.

Figure 6 shows the threshold voltage as a function of the inclination angle for channel lengths of 200 and 400 nm and for doping concentrations of $10^{15}$, $10^{16}$, and $10^{17}$ cm$^{-3}$. For this data set, the angle variation was obtained through the variation of the top silicon width, whereas the base silicon width and silicon height were maintained constant at 50 and 100 nm, respectively.

The short-channel effect (SCE) can be observed for all devices simulated, comparing the $L = 200$ nm to the $L = 400$ nm curves. When the inclination angle ($\theta$) decreases, the SCE becomes worse because of the rise of silicon width at the top of the device, which implies less gate/channel control. The length of 400 nm is adopted for the study of the impact of the inclination angle ($\theta$) over the threshold voltage, because the SCE is less significant.

It can also be observed in Fig. 5 and 6 that the slope of $V_{th} \times \theta$ inclination angle depends on the doping level. The physical reason for this dependence is the silicon-film composition of charge. Actually, the composition of charge (depletion charge and inversion charge) in the silicon film has a strong influence on the threshold-voltage behavior. Figure 7 shows the electron-concentration profile at half-length plane ($L/2$) in the silicon film at $V_{GS} = V_{th}$ for two doping levels and two silicon fin widths. For both doping levels, the electron concentration is above $10^{16}$ cm$^{-3}$, and for devices with a width of 30 nm, the electron concentration is near $10^{17}$ cm$^{-3}$. This means that, while the silicon-film charge is mostly composed of depletion charge for the device with a doping level of $10^{17}$ cm$^{-3}$, the charge is predominantly composed of minority carriers, because the depletion charge

![Figure 2](image1.png)

**Figure 2.** Electron concentration isosurface from numeric three-dimensional simulation showing corner effect. $V_{Fin} = 0.05$ V, $V_{Gst} = 0.42$ V, $t_{box} = 100$ nm, and $L = 200$ nm.

![Figure 3](image2.png)

**Figure 3.** FinFET cross-sectional shapes: (a) trapezoidal, (b) concave, (c) convex, and reference angle $\theta$.

![Figure 4](image3.png)

**Figure 4.** Simulated device. $t_{ox}$—gate-oxide thickness. $t_{box}$—buried-oxide thickness. $W_{Fin}$—silicon film width (bottom and top). $H_{Fin}$—Fin height. $\theta$—inclination angle. $L$—channel length.

![Figure 5](image4.png)

**Figure 5.** FinFET’s second derivative of $I_{DS} \times V_{Gst}$ curves for some $\theta$ values and for doping concentrations of $10^{15}$, $10^{16}$, and $10^{17}$ cm$^{-3}$.
density is limited to $10^{15}$ cm$^{-3}$. An immediate consequence of this different distribution of charge can be observed in the volume-inversion mechanism, which is more visible in the lightly doped device. As the doping level becomes higher, the carrier concentration rises near the silicon-oxide surface and decreases in the middle of the device. In an extreme situation the device could even approach partial depletion. In such a case, the potential profile would be nearly parabolic, and the threshold-voltage expression would be dominated by a term directly proportional to the fin width. This simulation results of Fig. 6, including the slope of $V_{th}$ expression is plotted as a function of silicon film width, for $N_A = 10^{17}$ through $2.5 \times 10^{17}$ cm$^{-3}$, $L = 400$ nm.

In Fig. 8, the resulting $V_{th}$ expression is plotted as a function of silicon film width for parallel-wall devices. The results for the $10^{17}$ doping level are close to those obtained in the three-dimensional simulation results of Fig. 6, including the slope of $V_{th}$ as $W_{fin}$. Unfortunately, this model has some restrictions due to the assumptions made for its derivation and cannot be applied to the lower doping levels simulated. The Appendix presents Francis’s model and restrictions.

Figure 6. FinFET’s threshold voltage as a function of $\theta$ for channel lengths of 200 and 400 nm and for doping concentrations of $10^{15}$, $10^{16}$, and $10^{17}$ cm$^{-3}$.

Figure 7. Electron concentration profile at the half-length ($L/2$) plane in the silicon film ($h = H_{fin}/2$, $\theta = 90^\circ$) at $V_G = V_{th}$ for FinFET width of 30 and 50 nm and doping concentrations of $10^{15}$ and $10^{17}$ cm$^{-3}$.

Figure 8. Francis’s model threshold-voltage levels for $\theta = 90^\circ$ as a function of silicon film width, for $N_A = 10^{17}$ through $2.5 \times 10^{17}$ cm$^{-3}$, $L = 400$ nm.
which some silicon regions are narrower than 10 nm. In these regions the quantum-confinement effects begin to play important roles in the device behavior, and none of the studied models could be applied without some further analysis.

Corner Effect Analysis

The corner effect is characterized by the increment of the inversion charge earlier in the corners than in other regions of the device. Three-dimensional simulation is especially useful to the corner-effect study, because the electric field and the carrier concentration can be observed in any device region. In this work, the carrier concentration was observed at the device cross section perpendicular to the gate planes, like in Fig. 2. The current direction is perpendicular to this plane. When the device is biased with a small drain-to-source voltage (0.05 V) and the gate-to-source voltage is increased, the channel inversion occurs first near the corners, then in the corner surroundings, and finally in the regions far from the corners. This occurs due to the higher electric field. In the corner region, the electric field is given by the sum of the influences of the electric fields of the adjacent gate planes. The current density across the perpendicular section is also higher at the corners for gate voltages near the device threshold. This regional inversion process cannot be directly observed in the current-voltage curves for the device parameters used in this work.

In order to evaluate the sidewall inclination-angle influence on the intensity of the corner effects, the electron concentration was chosen as an electrostatic parameter. A set of devices with different sidewall inclination angles and different doping levels was simulated under the same bias: \( V_{DS} = 0.05 \) V and \( V_{GF} = 0.44 \) V. The basic device for simulation is a trapezoidal cross-sectional triple-gate FinFET, as shown in Fig. 2. The geometric parameters and main physical dimensions are defined as for the double-gate device of Fig. 5. For convex and concave shapes, the sidewall geometry near the corners is locally approximated by a tangent plane, with the angle defined as in Fig. 1. The simulated devices present gate-oxide thicknesses \( t_{ox} = 2 \) nm, buried-oxide thicknesses \( t_{box} = 100 \) nm, silicon doping concentration \( N_{a} \) ranging from \( 10^{15} \) to \( 10^{17} \) cm\(^{-3}\), and interface charge densities of \( 3.0 \times 10^{10} \) cm\(^{-2}\). The channel length \( L \) is 200 nm. The three-dimensional simulator used was Atlas.\(^{11}\) The angle (\( \theta \)) variation was obtained through the variation of the top silicon width \( W_{Fin, top} \) from 30 to 70 nm, while the bottom silicon width \( W_{Fin, bottom} \) and the silicon height \( H_{silicon} \) were maintained constant at 50 nm. The inclination angle \( \theta \) ranged from \(-11^\circ\) to \(11^\circ\). Negative angles occur when the trapezoid top is larger than the bottom.

The electron concentration data of the cross section located \( L/2 \) far from the drain were observed and the maximum value, which occurs at the top corner, was taken for each device. The results are plotted in Fig. 10, as functions of the sidewall inclination angle, for doping levels of \( 10^{15} \), \( 10^{16} \), \( 10^{17} \), and \( 5 \times 10^{17} \) cm\(^{-3}\). For smaller angles, the electron concentration is higher, and consequently the corner effect is also higher. This result can be explained by the fact that, for smaller and especially for negative angles, the region near the corner is better coupled to the gate planes than to the other fixed potentials of the structure (drain, source, and substrate). As this angle is increased, the corner region is exposed to the influences of these other potentials. It can also be seen in Fig. 10 that, comparing the four curves of the four simulated doping levels, the corner effect is less meaningful at lower doping levels. This is a reasonable result, because the carrier distribution along the cross section of less-doped devices is more uniform and a large part of the carrier is not close to the silicon/gate-oxide interface and consequently not close to the corners. For the same reason, the slope of these curves also depends on the doping level; the higher the doping level, the higher the influence of the gate coupling over the charge distribution and the higher the \( \theta \) angle influence on the corner effects.

Although the electron concentration is a good parameter for the corner-effect analysis, once it is directly related to the effect, it is important to analyze the consequences on the current distribution. The current density was observed at the same cross section as in the static analysis and for the same simulated devices. The chosen parameter for the dynamic analysis was the ratio between the maximum current density observed in the cross-section simulation nodes and the average current density in the same cross section, under the same bias, calculated by Expression 2

\[
J_N = \frac{J_{max}}{I_{DS}/A}
\]  

where \( J_N \) is the normalized current density, \( J_{max} \) is the maximum current density observed in the cross section, \( I_{DS} \) is the drain-to-source current, and \( A \) is the cross-section area. The results obtained are plotted in Fig. 11. The current behavior is coherent with the charge distribution; when there is a greater concentration of carriers at the corners, the current also grows. This coherence can be observed in the angle dependence as well as in the doping-concentration dependence. As observed in the electron-concentration analysis, the strongest corner effect occurs for the smaller angle \((-11^\circ)\) and for the higher doping level \((5 \times 10^{17} \) cm\(^{-3}\))

Besides the top-corner effects, a similar phenomenon takes place at the bottom corners. It is caused by the discontinuity (edge) of the lateral gate electrodes and the sum of electric fields of the lateral gate and the substrate. The static and dynamic observations were made through the same parameters used in the top-corner effect analysis, the electron concentration and relative maximum current density \( J_N \). The results are presented in Fig. 12 and 13. The simulated devices are the same as those used for the top-corner analysis.
The angle \( \theta \) is defined in the same way as in the preceding analysis (see Fig. 3), but, considering the geometry of the device, it is important to emphasize that when \( \theta \) is increased, the top-corner angle is also increased, and the bottom-corner angle is decreased. The bottom-corner effect dependence on the sidewall angle is related to the coupling between the channel region and the lateral gate electrode. For greater distances (smaller trapezium bottom angle), the distance between the channel and the gate electrode is smaller, which implies better coupling and higher corner effects. This behavior can be observed in Figs. 12 and 13.

The maximum relative current density and the maximum electron density at the top of the devices decreases as the sidewall inclination angle increases. The bottom-corner effect has a weaker dependence on the inclination angle than the top.

Comparing the simulated doping levels, it can be seen that the corner effect is less significant at lower doping levels. This fact occurs because the current distribution along the cross section of such devices is more uniform and a large part of the current flows far from the silicon/gate-oxide interface, and consequently far from the corners.

Conclusions

A set of dual-gate and triple-gate trapezoidal FinFETs with different sidewall inclination angles was simulated using a three-dimensional numeric device simulator. The sidewall inclination-angle influences on the threshold voltage, on the body electron concentration, and on the current distribution were evaluated. The maximum relative current density and the maximum electron density were adopted as comparison factors for the corner-effect intensity. The results show that the inclination angle affects these device characteristics in different ways, depending on the body doping level. Threshold voltage rises as the angle increases for higher doping levels and decreases for smaller doping levels. The corner effect at the top of the devices decreases as the sidewall inclination angle increases. The bottom-corner effect has a weaker dependence on the inclination angle than the top.

References